

**JNTUA COLLEGE OF ENGINEERING (Autonomous), ANANTHAPURAMU**  
**Department of Electronics & Communication Engineering**  
**M. Tech (Regular) – VLSI SYSTEM DESIGN(VLSI SD)**  
**(w. e. f 2016-17 Admitted Batch )**

**COURSE STRUCTURE**

**M. Tech I Semester**

S.No	Sub. Code	Subject	Theory	Lab	Credits
1.	16D43101	Digital System Design	4	-	4
2.	16D43102	VLSI Technology and Design	4	-	4
3.	16D43103	CMOS Analog IC Design	4	-	4
4.	16D43104	CMOS Digital IC Design	4	-	4
5.	16D43105	<b>Elective-I</b> a) Analysis and Design of Digital Systems Through Verilog HDL	4	-	4
	15D41103	b) Advanced Computer Architecture			
	16D43106	c) CAD for VLSI			
6.	15D41206	<b>Elective-II</b> a) CPLD and FPGA Architectures and Applications	4	-	4
	16D43107	b) Linux Programming & Scripting Languages			
	16D43108	c) Optimization Techniques in VLSI Design			
7.	16D43109	VLSI System Design Lab	-	3	2
Contact periods/week			<b>24</b>	<b>03</b>	<b>26</b>
			Total/week	<b>27</b>	

**M. Tech II Semester**

S.No	Sub. Code	Subject	Theory	Lab	Credits
1.	15D41205	Low Power VLSI Design	4	-	4
2.	16D43201	CMOS Mixed Signal Design	4	-	4
3.	15D41201	Embedded System Design	4	-	4
4.	15D41211	Test and Testability	4	-	4
5.	16D43202	<b>Elective-III</b> a) System On chip Architectures	4	-	4
	16D43203	b) Semiconductor Memory Design and Testing			
	16D43204	c) Design for Testability			
6.	16D43205	<b>Elective-IV</b> a) System Verilog	4	-	4
	16D43206	b) VLSI Signal Processing			
	16D43207	c) Physical Design Automation			
7.	15D54201	Research Methodology (Audit Course)	2	-	-
8.	16D43108	System Verification Lab	-	3	2
Contact periods/week			<b>26</b>	<b>03</b>	<b>26</b>
			Total/Week	<b>29</b>	

**M.Tech III & IV SEMESTERS**

<b>Code</b>	<b>Name of the Subject</b>	<b>C</b>
	<b>III Semester</b> Seminar- I	2
	<b>IV Semester</b> Seminar- II	2
	<b>III &amp; IV Semester</b> PROJECT WORK	44
	<b>Total</b>	<b>48</b>

**JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS): ANANTHAPURAMU  
VLSI SYSTEM DESIGN**

**(16D43101) DIGITAL SYSTEM DESIGN**

**M.Tech I Sem**

<b>T</b>	<b>P</b>	<b>C</b>
<b>4</b>	<b>0</b>	<b>4</b>

**Learning Outcomes:**

After completion of this course the students will be able to

- Complete knowledge regarding the minimization procedures employed in digital systems
- Apply minimization procedures for solving real world problems
- Build fault models for testing combinational and sequential circuits and Design fault models for testing digital systems
- Analyze different minimization procedures and fault models that are used with digital systems

**UNIT-I**

**Minimization Procedures and CAMP Algorithm** Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs., CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

**UNIT-II**

**PLA Design, PLA Minimization and Folding Algorithms** Introduction to PLDs, basic configurations and advantages of PLDs, PLA Introduction, Block diagram of PLA, size of PLA, LA design aspects, PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

**UNIT-III**

**Design of Large Scale Digital Systems** Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

**UNIT-IV**

**Fault Diagnosis in Combinational Circuits** Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

**UNIT-V**

**Fault Diagnosis in Sequential Circuits** Fault detection and location in sequential circuits, circuit test approach, initial state identification, Hamming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

**TEXTBOOKS:**

1. Logic Design Theory-N. N. Biswas, PHI
2. Switching and Finite Automata Theory-Z. Kohavi , 2nd Edition, 2001,TMH
3. Digital system Design using PLDd-Lala

**REFERENCE BOOKS:**

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

**JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS): ANANTHAPURAMU  
VLSI SYSTEM DESIGN**

**(16D43102) VLSI TECHNOLOGY AND DESIGN**

**M.Tech I Sem**

<b>T</b>	<b>P</b>	<b>C</b>
<b>4</b>	<b>0</b>	<b>4</b>

**Course Outcomes:**

After completion of the course the students will be able to

- Understand the fundamentals of CMOS VLSI design, and various electrical properties of MOS, BiCOMOS circuits
- Derive the expressions for various electrical properties of CMOS and BiCMOS circuits.
- Design small sub circuits using VLSI design technologies, FPGA, SoC.
- Analyze design concepts of combinational and sequential circuits

**UNIT-I**

**VLSI Technology:** Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.

**CMOS VLSI Design:** MOS Technology and fabrication process of pMOS, nMOS, CMOS and BiCMOS technologies, comparison of different processes.

**UNIT-II**

Building Blocks of a VLSI circuit: Computer architecture, memory architectures, communication interfaces, mixed signal interfaces. VLSI Design Issues: Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

**UNIT-III**

**Basic electrical properties of MOS and BiCMOS circuits:** MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitative and quantitative analysis with proper illustrations and necessary derivations of expressions.

**UNIT-IV**

**Subsystem Design and Layout:** Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations. Subsystem Design Processes: Some general considerations and an illustration of design processes, design of an ALU subsystem.

**UNIT-V**

**Floor Planning:** Introduction, Floor planning methods, off-chip connections. Architecture Design: Introduction, Register-Transfer design, high-level synthesis, architectures for low power, architecture testing. Chip Design: Introduction and design methodologies.

**TEXT BOOKS:**

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell, Sholeh Eshraghian, 2005, PHI Publications.
2. Modern VLSI Design-Wayne Wolf, 3<sup>rd</sup> Ed., 1997, Pearson Education.

**REFERENCE BOOKS:**

1. VLSI Design Technologies for Analog and Digital Circuits, Randall L.Geiger, Phillip E.Allen, Noel R.Strader, TMH Publications, 2010.
2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming-BO Lin, CRC Press, 2011.
3. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2<sup>nd</sup> Edition, Addison Wesley
4. VLSI Design-Dr.K.V.K.K.Prasad, Kattula Shyamala, Kogent Learning Solutions Inc., 2012

**JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS): ANANTHAPURAMU  
VLSI SYSTEM DESIGN**

**(16D43103) CMOS ANALOG IC DESIGN**

**M.Tech I Sem**

<b>T</b>	<b>P</b>	<b>C</b>
<b>4</b>	<b>0</b>	<b>4</b>

**Course Outcomes:**

After completion of the course the students will be able to

- Understand significance of different biasing styles and apply them for designing analog ICs.
- Analyze the functionality of Current Mirrors, Current Sinks, Differential amplifiers and Current amplifiers.
- Design basic building blocks of analog ICs like, current mirrors, current sources, current sinks, two stage CMOS Power amplifiers and comparators.

**UNIT –I**

**MOS Devices and Modeling:** The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

**UNIT –II**

**Analog CMOS Sub-Circuits:** MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

**UNIT –III**

**CMOS Amplifiers:** Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures, Mismatch-offset cancellation techniques, Reduction of Noise by offset cancellation techniques, Alternative definition of CMRR.

**UNIT –IV**

**CMOS Operational Amplifiers:** Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

**UNIT –V**

**Comparators:** Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

**TEXT BOOKS:**

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

**REFERENCE BOOKS:**

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.
2. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce,
3. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.



**JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS): ANANTHAPURAMU  
VLSI SYSTEM DESIGN**

**(16D43104) CMOS DIGITAL IC DESIGN**

**M.Tech I Sem**

<b>T</b>	<b>P</b>	<b>C</b>
<b>4</b>	<b>0</b>	<b>4</b>

**Course Outcomes:**

After completion of the course the students will be able to

- Design CMOS inverters with specified noise margins and propagation
- Complete knowledge regarding the different issues associated with organization and design of semiconductor memories
- Realize and implement basic combinational and sequential elements that are commonly observed in digital ICs.
- Design basic combinational and sequential elements using NMOS and CMOS design strategies.
- Analyze the dynamic performance of CMOS circuits

**UNIT-I**

**MOS Design Pseudo NMOS Logic:** Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

**UNIT-II**

**Combinational MOS Logic Circuits:** MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

**UNIT-III**

**Sequential MOS Logic Circuits:** Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

**UNIT-IV**

**Dynamic Logic Circuits:** Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

**UNIT-V**

**Semiconductor Memories:** Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash

**TEXT BOOKS:**

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

**REFERENCE BOOKS:**

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

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VLSI SYSTEM DESIGN**

**ELECTIVE-I**

**(16D43105) ANALYSIS AND DESIGN OF DIGITAL SYSTEMS THROUGH  
VERILOG HDL**

**M.Tech I Sem**

<b>T</b>	<b>P</b>	<b>C</b>
<b>4</b>	<b>0</b>	<b>4</b>

**Course Outcomes:**

After completion of the course the students will be able to

- Understand syntax of various commands available with verilog and fundamental associated with design of digital systems
- To design and simulate sequential and concurrent techniques in verilog and explain modeling of digital systems using verilog and design methodology
- Able develop problem solving skills and adapt them to solve real world problems
- Use computer as tool for solving research issues

**UNIT-I**

**Digital Logic Design using Verilog HDL Introduction:** Verilog Data types and Operators, Binary data manipulation, Combinational and Sequential logic design, Structural Models of Combinational Logic, Logic Simulation, Design Verification and Test Methodology, Propagation Delay, Truth Table models using Verilog.

**UNIT-II**

**Combinational Logic Circuit Design using Verilog:** Combinational circuits building blocks: Multiplexers, Decoders , Encoders , Code converters, Arithmetic comparison circuits , Verilog for combinational circuits , Adders-Half Adder, Full Adder, Ripple-Carry Adder, Carry Look-Ahead Adder, Subtraction, Multiplication.

**UNIT-III**

**Sequential Logic Circuit Design using Verilog:** Flip-flops, registers & counters, synchronous sequential circuits: Basic design steps, Mealy State model, Design of FSM using CAD tools, Serial Adder Example, State Minimization, Design of Counter using sequential Circuit approach.

**UNIT-IV**

**Digital Logic Circuit Design Examples using Verilog:** HDL Behavioral modeling , Data types, Boolean-Equation-Based behavioral models of combinational logics , Propagation delay and continuous assignments, latches and level-sensitive circuits in Verilog, Cyclic behavioral models

of flip-flops and latches and Edge detection, comparison of styles for behavioral model; Behavioral model, Multiplexers, Encoders and Decoders, Counters, Shift Registers, Register files, Dataflow models of a linear feedback shift register, Machines with multi cycle operations,

**UNIT-V**

**ASM and ASMD charts for behavioral modeling:** Design examples, Keypad scanner and encoder. Synthesis of Digital Logic Circuit Design Introduction to Synthesis, Synthesis of combinational logic, Synthesis of sequential logic with latches and flip-flops, Synthesis of Explicit and Implicit State Machines, Registers and counters.

**TEXT BOOKS:**

1. Stephen Brown & Zvonko Vranesic, “Fundamentals of Digital logic design with Verilog”, Tata McGraw Hill, 2<sup>nd</sup> edition.
2. Michael D. Ciletti, “Advanced digital design with the Verilog HDL”, Eastern economy edition, PHI.

**REFERENCE BOOKS:**

1. Stephen Brown & Zvonko Vranesic, “Fundamentals of Digital logic with Verilog design”, Tata McGraw Hill, 2<sup>nd</sup> edition.
2. Bhaskar, “Verilog Primer”, 3<sup>rd</sup> Edition, PHI Publications.
3. Z.Navabi, VHDL Analysis and Modeling of Digital Systems, (2/e), McGraw Hill, 1998.
4. Douglas Perry, VHDL (3/e), McGraw Hill. 2002

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**ELECTIVE-I**

**M.Tech I Sem**

<b>T</b>	<b>P</b>	<b>C</b>
<b>4</b>	<b>0</b>	<b>4</b>

**(15D41103) ADVANCED COMPUTER ARCHITECTURE**

**Course objective:**

- To study about various parallel computer models and also to study the program and network properties
- To study the concepts of pipelining and super scalar techniques.
- To study about architectures of multi processors and multi computers

**Course Outcome:**

After completion of the course the students will be able to

- Know about different parallel computer models and their network properties.
- Understand about different concepts related to pipelining and super scalar techniques.
- Get complete knowledge regarding multi processors and multi computers.

**UNIT - I**

**Parallel Computer Models** – System attributes to performance, Multiprocessors and Multicomputers, Classifications of Architectures, Multivector and SIMD Computers, Architecture development tracks

**UNIT - II**

**Program and Network Properties-** Conditions for parallelism, Program partitioning and Scheduling, Program flow mechanisms, System interconnect architectures, Performance metrics and measures, Parallel Processing Applications

**UNIT-III**

**Processors and Memory Hierarchy-** Advanced Processor Technology, Superscalar and Vector processors, Memory hierarchy technology, Virtual Memory, Backplane bus systems, Cache memory organizations, Shared memory organizations

**UNIT - IV**

**Pipelining and Superscalar Techniques** Linear Pipeline processors, Nonlinear pipeline processors, Instruction pipeline design, Arithmetic pipeline design, Superscalar and Super Pipeline Design

**UNIT- V**

**Multiprocessors and Multicomputers** Multiprocessor System Interconnects, Cache Coherence and Synchronization mechanisms, Three generations of Multicomputers, Message passing mechanisms, Vector Processing principles, Principles of Multithreading

**Text Books:**

1. Hwang kai, "Advanced Computer Architecture", McGraw-Hill, 2001.
2. Patterson, David and Hennessy John, Morgan Kaufmann, "Computer Architecture", 2001.

**References:**

1. William Stallings, Computer Organization and Architecture, 8th Edition, Prentice-Hall India, 2010.
2. David A Patterson and John L. Hennessy, Computer Organization and Design, 4th Edition, Elsevier India, 2011.
3. Andrew S Tanenbaum and James R Goodman, Structured Computer Organization, 5th Edition PrenticeHall India, 2009.

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VLSI SYSTEM DESIGN**

**ELECTIVE-I**

**(16D43106) CAD FOR VLSI DESIGN**

**M.Tech II Sem**

<b>T</b>	<b>P</b>	<b>C</b>
<b>4</b>	<b>0</b>	<b>4</b>

**UNIT-I**

VLSI Physical Design Automation VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

**UNIT-II**

Partitioning, Floor Planning, Pin Assignment and Placement Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing,

Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments,

**UNIT-IV**

Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

Global Routing and Detailed Routing Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

**UNIT-V**

Physical Design Automation of FPGAs and MCMs FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

**TEXT BOOKS:**

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3<sup>rd</sup> Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3<sup>rd</sup> Ed., 2011.

**REFERENCE BOOKS:**

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition



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**ELECTIVE-II**

**(15D41206) CPLD AND FPGA ARCHITECTURES AND APPLICATIONS**

**M.Tech II Sem**

<b>T</b>	<b>P</b>	<b>C</b>
<b>4</b>	<b>0</b>	<b>4</b>

**UNIT-I**

**Introduction to Programmable Logic Devices** Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

**UNIT-II**

**Field Programmable Gate Arrays** Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

**UNIT-III**

**SRAM Programmable FPGAs** Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

**UNIT-IV**

**Anti-Fuse Programmed FPGAs** Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

**UNIT-V**

**Design Applications** General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

**TEXT BOOKS:**

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

**REFERENCE BOOKS:**

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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**VLSI SYSTEM DESIGN**

**ELECTIVE II**

**(16D43107) LINUX PROGRAMMING & SCRIPTING LANGUAGE**

**M.Tech I Sem**

<b>T</b>	<b>P</b>	<b>C</b>
<b>4</b>	<b>0</b>	<b>4</b>

After completion of the course the students will be able to

- Understand basic commands of Linux that are required to work with linux.
- Understand basic commands of perl.
- Write scripts using perl for building CMOS desing

**UNIT-I**

**Linux Basics:** Introduction to Linux, File System of the Linux, General usage of Linux kernel 7 basic commands, Linux users and group, Permissions for file, directory and users, Searching a file & directory, Zipping and unzipping concepts.

**UNIT-II**

**Overview of scripting language:** PERL, File handles, Operators, Control structures, Regular expressions, Built in data types, Operators, Statements and declarations- simple, Compound, Loop statements, Global and scoped declarations.

**UNIT-III**

**Pattern matching:** Regular expression, Pattern matching operators, Character classes, Positions, capturing and clustering.

**UNIT-IV**

PERL built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

**UNIT-V**

**Threads:** Process model, Thread model, Perl debugger, Using debugger commands, Customization, Internals and externals, Internal data types, Extending perl, embedding perl, Exercises for programming using perl.

**TEXT BOOKS:**

1. Randal L, Schwartz Tom Phoenix, "Learning PERL", O'Reilly Publications, 3rd Edn., 2000
2. Larry Wall, Tom Christiansen, John Orwant, "Programming PERL", O'Reilly Publications, 3rd Edn., 2000.

**REFERENCE BOOKS:**

1. Linux LRM.

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VLSI SYSTEM DESIGN**

**ELECTIVE II**

**(16D43108) OPTIMIZATION TECHNIQUES IN VLSI DESIGN**

**M.Tech I Sem**

<b>T</b>	<b>P</b>	<b>C</b>
<b>4</b>	<b>0</b>	<b>4</b>

**Course Outcomes:**

After completion of the course the students will be able to

- Understand basics of statistical modeling
- Analyze performance of CMOS circuits with respect to power, area and speed
- Gets complete knowledge regarding the various algorithms used for optimization of power and area.

**UNIT-I**

**Statistical Modeling:** Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

**UNIT-II**

**Statistical Performance, Power and Yield Analysis** Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

**UNIT-III**

**Convex Optimization** Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Polynomial fitting.

**UNIT-IV**

**Genetic Algorithm** Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement GASP algorithm-unified algorithm.

**UNIT-V**

**GA Routing Procedures and Power Estimation** Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

**TEXT BOOKS:**

1. Statistical Analysis and Optimization for VLSI: Timing and Power -Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation -Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.

**REFERENCE BOOKS:**

1. Convex Optimization - Stephen Boyd, Lieven Vandenberghe, Cambridge University Press,2004.

**JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS): ANANTHAPURAMU  
VLSI SYSTEM DESIGN**

**(16D43109) VLSI SYSTEM DESIGN LAB**

**M.Tech I Sem**

<b>T</b>	<b>P</b>	<b>C</b>
<b>0</b>	<b>3</b>	<b>2</b>

**Learning Outcomes:**

After completion of this course the students will be able to

- Understand syntax of various commands available with verilog and fundamental associated with design of digital systems
- To design and simulate and implement various digital system like traffic light controller, UART.
- Able develop problem solving skills and adapt them to solve real world problems
- Write scripts using perl for building digital blocks

The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter
4. Single Port Synchronous RAM.
5. Synchronous FIFO.
6. ALU.
7. UART Model.
8. Dual Port Asynchronous RAM.

9. Fire Detection and Control System using Combinational Logic circuits.
10. Traffic Light Controller using Sequential Logic circuits
11. Pattern Detection using Moore Machine.
12. Finite State Machine (FSM) based logic circuit.
13. Perl Programming for basic operations.

**Lab Requirements:****Software:**

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Quarta Simulator, Mentor Graphics-Precision RTL, Perl Software.

**Hardware:**

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.



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**(15D41205) LOW POWER VLSI DESIGN**

After the completion of the course students will be able to

- Under stand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
- Implement Low power design approaches for system level and circuit level measures.
- Design low power adders, multipliers and memories for efficient design of systems.

Fundamentals Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

**UNIT –II**

Low-Power Design Approaches Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches System Level Measures, Circuit Level Measures, Mask level Measures.

**UNIT –III**

Low-Voltage Low-Power Adders Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

**UNIT –IV**

Low-Voltage Low-Power Multipliers Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

**UNIT –V**

Low-Voltage Low-Power Memories Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

**TEXT BOOKS**

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

**REFERENCE BOOKS**

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

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**(16D43201)CMOS MIXED SIGNAL DESIGN**

After the Completion of the course the students will be able to

- Demonstrate first order filter with least interference
- Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
- Design different A/D, D/A, modulators, demodulators and different filter for real time applications

**UNIT-I**

Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

**UNIT-II**

Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs- Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

**UNIT-III**

Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

**UNIT-IV**

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time- interleaved converters.

**UNIT-V**

Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

**TEXT BOOKS:**

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013

**REFERENCE BOOKS:**

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009

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**(15D41201)EMBEDDED SYSTEM DESIGN**

**Course Outcome:**

After completion of this course the students will be able to understand

- The issues relating to hardware and software design concepts associated with processor in Embedded Systems.
- The concept of low power microcontrollers.
- The hardware software co- design issues pertaining to design of an Embedded System using low power microcontrollers.

**UNIT – I**

**Introduction to Embedded Electronic Systems and Microcontrollers:**

An Embedded System-Definition, Embedded System Design and Development Life Cycle, An Introduction to Embedded system Architecture, The Embedded Systems Model, Embedded Hardware: The Embedded Board and the von Neumann Model, Embedded Processors: ISA Architecture Models, Internal Processor Design, Processor Performance, Board Memory: Read-Only Memory (ROM), Random-Access Memory (RAM), Auxiliary Memory, Memory Management of External Memory and Performance, Approaches to Embedded Systems, Small Microcontrollers, Anatomy of a Typical Small Microcontroller, Small Microcontrollers Memory, Embedded Software, Introduction to small microcontroller (MSP430).

**UNIT-II**

**MSP430 – I:**

**Architecture of the MSP430 Processor:** Central Processing Unit, Addressing Modes, Constant Generator and Emulated Instructions, Instruction Set, Examples, Reflections on the CPU and Instruction Set, Resets, Clock System, Memory and Memory Organization.

**Functions, Interrupts, and Low-Power Mode:** Functions and Subroutines, Storage for Local Variables, Passing Parameters to a Subroutine and Returning a Result, Mixing C and Assembly Language, Interrupts, Interrupt Service Routines, Issues Associated with Interrupts, Low-Power Modes of Operation.

**UNIT – III**

**MSP430 – II:**

**Digital Input, Output, and Displays:** Parallel Ports, Digital Inputs, Switch Debounce, Digital Outputs, Interface between Systems, Driving Heavier Loads, Liquid Crystal Displays, Simple Applications of the LCD.

**Timers:** Watchdog Timer, Timer\_A, Timer\_A Modes, Timer\_B, Timer\_B Modes, Setting the Real-Time Clock, State Machines.

**UNIT – IV**

**MSP430 Communication:**

Communication Peripherals in the MSP430, Serial Peripheral Interface, SPI with the USI, SPI with the USCI, A Thermometer Using SPI Modes, Inter-integrated Circuit Bus (I<sup>2</sup>C) and its operations, State Machines for I<sup>2</sup>C Communication, A Thermometer Using I<sup>2</sup>C, Asynchronous Serial Communication, Asynchronous Communication with the USCI\_A, A Software UART Using Timer\_A, Other Types of Communication.

**UNIT – V****MSP430 Case Studies:**

Introduction to Code Composer studio (CC Studio Ver. 6.1) a tutorial, A Study of blinking LED, Enabling LED using Switches, UART Communication, LCD interfacing, Interrupts, Analog to Digital Conversion, General Purpose input and output ports, I<sup>2</sup>C.

**Text Books:**

1. Tammy Noergaard “Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers”, Elsevier (Singapore) Pvt. Ltd. Publications, 2005.
2. John H. Davies “MSP430 Microcontroller Basics”, Elsevier Ltd Publications, Copyright 2008.

**References:**

1. Manuel Jiménez Rogelio, Palomera Isidoro Couvertier “Introduction to Embedded Systems Using Microcontrollers and the MSP430” Springer Publications, 2014.
2. Frank Vahid, Tony D. Givargis, “Embedded system Design: A Unified Hardware/Software Introduction”, John Wiley & Sons Inc. 2002.
3. Peter Marwedel, “Embedded System Design”, Science Publishers, 2007.
4. Arnold S Burger, “Embedded System Design”, CMP Books, 2002.
5. Rajkamal, “Embedded Systems: Architecture, Programming and Design”, TMH Publications, Second Edition, 2008.

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**(15D41211)TESTING AND TESTABILITY**

**Course Outcome:**

After completion of this course the students will be able to

- Understand different types of faults associated with logic circuits and types of testing by employing fault models to the logic circuits.
- Study about different methods of simulation and algorithms associated with testing.
- Get complete knowledge about different methods of simulation and algorithms associated with testing.

**UNIT-I: Introduction to Testing**

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

**UNIT-II: Logic and Fault Simulation**

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

**UNIT -III: Testability Measures**

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

**UNIT-IV: Built-In Self-Test**

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

**UNIT-V: Boundary Scan Standard**

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

**References:**

1. M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Publishers.
2. M. Abramovici, M.A.Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House.
3. P.K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

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**ELECTIVE-III**

**(16D43202) SOC ARCHITECTURES**

***Course Outcome:***

After completion of this course the students will be able to

- Get complete basics related to SoC architecture and different approaches related to SoC Design.
- Able to select an appropriated robust processor for SoC Design
- Able to Select an appropriate memory for SoC Design.
- Design SoC
- Realize real time case studies

**UNIT I:**

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

**UNIT II:**

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

**UNIT III:**

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

**UNIT IV:**



Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

**UNIT V:**

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

**TEXT BOOKS:**

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiley India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2<sup>nd</sup> Ed., 2000, Addison Wesley Professional.

**REFERENCE BOOKS:**

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers

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**ELECTIVE-III**

**(16D43203) SEMICONDUCTOR MEMORY DESIGN AND TESTING**

After completion of the course the students will be able to

- Get complete knowledge regarding different types of memories, their architectural and different packing techniques of memories.
- Able to build fault models for memory testing.
- Analyze different parameters that leads malfunctioning of memories.
- Design reliable memories with efficient architecture to improve processes times and power

**UNIT-I**

**Random Access Memory Technologies** SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

**UNIT-II**

**Non-volatile Memories** Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

**UNIT-III**

**Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance** RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

**UNIT-IV**

**Semiconductor Memory Reliability and Radiation Effects** General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

**UNIT-V**

**Advanced Memory Technologies and High-density Memory Packing Technologies** Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

**TEXT BOOKS:**

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.

**REFERENCE BOOKS:**

1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice all.

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**ELECTIVE-III**

**(16D43204)DESIGN FOR TESTABILITY**

***Course Outcome:***

After completion of the course the student will be able to

- Get complete knowledge on different types of faults, fault models and different algorithms that can be employed for fault modeling.
- Built different fault models and analyze the using testability measures
- Design different types of built in self test pattern generators which aid for design of fault tolerant systems

**UNIT-I**

Introduction to Testing Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

**UNIT-II**

Logic and Fault Simulation Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

**UNIT –III**

Testability Measures SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

**UNIT-IV**

Built-In Self-Test The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

**UNIT-V**

Boundary Scan Standard Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

**TEXT BOOKS:**

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Publishers.

**REFERENCE BOOKS:**

1. Digital Systems and Testable Design - M. Abramovici, M.A. Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

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**ELECTIVE-IV**

**(16D43205)SYSTEM VERILOG**

***Course Outcome:***

After completion of the course the student will be able to

- Get complete knowledge on principles of verification, and usage of System Verilog for verification
- Write test benches different layered architectures using system verilog
- Verify the functionality of different complex logics

**UNIT 1**

**Verification Concepts:** Importance of Verification, Concepts of Verification. Functional Verification process. Verification plan, Stimulus Generation. Test bench Generation, components and their performance, Coverage: Code and Functional coverage.

**UNIT II**

**System Verilog – 1:** Introduction to SV : Language evolution. Classes and objects. Class Variables and Methods. Class instantiation. Constructors. Inheritance. Derived classes. Data hiding and encapsulation. Polymorphism. System Verilog constructs - Data types: bit data, strings, arrays : queues, dynamic and associative arrays. New type creation. Structs, enumerated types. Routines for enumerated types. Statements. Procedural, continue and break statements. Tasks and functions. structures and unions, casting, Operators, Loops, Jumps, Program blocks. Processes and threads. IPC. Mailboxes and semaphore

**UNIT III**

**System Verilog – 2:** Modules, ports and interfaces. Communication with ports. Grouping signals. Clocking Blocks. Classes, Class Variables. Directed Vs Random Testing. Randomization. Constraint Driven Randomization. Coverage driven verification : Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.

**UNIT IV**

**Layered Test bench Architecture For Verification:** Layered Test benches. Stimulus and Response.

Necessity for methodology. Verification Planning. Test bench architecture & Environment configuration : Generator, Driver, Receiver, Score board. assertions: Introduction to Assertion based verification, Immediate and concurrent assertions. Sequences and Assertion coverage

#### **UNIT V**

**Verification of Architectural Building Blocks / Sub-Systems:** Verification of Architectural building blocks and sub systems using system verilog: arbitration modules, arithmetic circuits, combinational and sequential blocks, data integrity, CDC, registers and memories.

#### **REFERENCES:**

1. Janick Bergeron, Writing Testbenches Using SystemVerilog
2. Chris Spear, SystemVerilog for Verification
3. Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale, Verification Methodology Manual for SystemVerilog

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**ELECTIVE-IV**

**(16D43206)VLSI SIGNAL PROCESSING**

***Course Outcomes:***

After completion of the course the students will be able to

- Get indepth knowledge on signal processing system and various techniques of power reduction.
- Realize various adders, multipliers and filters and optimize their operation of by reducing the redundant operations
- Apply concept of pipelined architecture for various combinational and sequential circuit modules like adders, multipliers, filters
- Design Low Power IIR filters

**UNIT-I**

Transformations for retiming. Folding and unfolding DSP programs.

**UNIT-II**

Bit level arithmetic structures- parallel multipliers, interleaved floor plan and bit plan based digital filters. Bit serial multipliers. Bit serial filter design and implementation . Canonic signed digit arithmetic, Distributed arithmetic.

**UNIT-III**

Redundant arithmetic, redundant number representations , carry free radix 2 addition and subtraction . Hybrid radix 4 addition. Radix 2 hybrid redundant multiplication architectures , data format conversion. Redundant to nonredundant converter. Numerical strength reduction.

**UNIT-IV**

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining. Implementation of wave-pipelined systems. Asynchronous pipelining.

**UNIT-V**

Scaling versus power consumption. Power analysis, power reduction techniques, power estimation techniques. Low power IIR filter design .Low power CMOS lattice IIR filter.



**Text Book:**

1. K.K. Parhi : VLSI Digital Signal Processing systems, John Wiley, 1999.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

**REFERENCE BOOKS:**

1. 2. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Mediseti V. K, 1995, IEEE Press (NY), USA.

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**ELECTIVE-IV****(16D43207) PHYSICAL DESIGN AUTOMATION*****Course Outcomes:***

After completion of the course the students will be able to

- Understand relation between automation algorithms and constraints posed by VLSI technology.
- Adopt algorithms to meet critical design parameters.
- Design area efficient logics by employing different routing algorithms and shape functions
- Simulate and synthesis different combinational and sequential logics

**UNIT-I**

**VLSI design automation tools:** algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools.

**UNIT-II**

**Layout** compaction, placement and routing, Design rules, symbolic layout. Applications of compaction. Formulation methods. Algorithms for constrained graph compaction. Circuit representation. Wire length estimation. Placement algorithms. Partitioning algorithms.

**UNIT-III**

**Floor planning and routing:** floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.

**UNIT-IV**

**Simulation and logic synthesis:** gate level and switch level modeling and simulation. Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.

**UNIT-V**

**High-level synthesis:** hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment and scheduling. Scheduling algorithms. Aspects of assignment. High level transformations.

**Text Books:**

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley ,1998.
2. N.A.Sherwani , Algorithms for VLSI Physical Design Automation, (3/e), Kluwer,1999.

**Reference Books:**

1. S.M. Sait , H. Youssef, VLSI Physical Design Automation, World scientific, 1999.
2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996

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**(15D54201) RESEARCH METHODOLOGY**  
**(Audit Course)**

**UNIT I**

Meaning of Research – Objectives of Research – Types of Research – Research Approaches – Guidelines for Selecting and Defining a Research Problem – research Design – Concepts related to Research Design – Basic Principles of Experimental Design.

**UNIT II**

Sampling Design – steps in Sampling Design – Characteristics of a Good Sample Design – Random Sampling Design.

Measurement and Scaling Techniques-Errors in Measurement – Tests of Sound Measurement – Scaling and Scale Construction Techniques – Time Series Analysis – Interpolation and Extrapolation.

Data Collection Methods – Primary Data – Secondary data – Questionnaire Survey and Interviews.

**UNIT III**

Correlation and Regression Analysis – Method of Least Squares – Regression vs Correlation – Correlation vs Determination – Types of Correlations and Their Applications

**UNIT IV**

Statistical Inference: Tests of Hypothesis – Parametric vs Non-parametric Tests – Hypothesis Testing Procedure – Sampling Theory – Sampling Distribution – Chi-square Test – Analysis of variance and Co-variance – Multi-variate Analysis.

**UNIT V**

Report Writing and Professional Ethics: Interpretation of Data – Report Writing – Layout of a Research Paper – Techniques of Interpretation- Making Scientific Presentations in Conferences and Seminars – Professional Ethics in Research.

**Text books:**

1. Research Methodology: Methods and Techniques – C.R.Kothari, 2<sup>nd</sup> Edition, New Age International Publishers.
2. Research Methodology: A Step by Step Guide for Beginners- Ranjit Kumar, Sage Publications (Available as pdf on internet)
3. Research Methodology and Statistical Tools – P.Narayana Reddy and G.V.R.K.Acharyulu, 1<sup>st</sup> Edition, Excel Books, New Delhi.

**References:**

1. Scientists must Write - Robert Barrass (Available as pdf on internet)
2. Crafting Your Research Future – Charles X. Ling and Quiang Yang (Available as pdf on internet)

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**(16D43108) SYSTEM VERIFICATION LAB**

**PART-A: VLSI Lab (Back-end Environment)**

The students are required to design and implement the Layout of the following experiments of any SIX using CMOS 130nm Technology.

**List of Experiments:**

1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Static RAM Cell.
6. Dynamic RAM Cell.
7. ROM
8. Digital-to-Analog-Converter.
9. Analog-to-Digital Converter.

**PART-B: Mixed Signal Simulation**

The students are required to perform the following experimental concepts with suitable complexity mixed-signal application based circuits of any FOUR (circuits consisting of both analog and digital parts) using necessary software tools.

**List of experimental Concepts:**

- Analog circuit simulation.
- Digital circuit simulation.
- Mixed signal simulation.
- Layout Extraction.
- Parasitic values estimation from layout
- Layout Vs Schematic.
- Net List Extraction.
- Design Rule Checks.

**Lab Requirements:**

**Software:** Xilinx ISE Suite 13.2 Version, Mentor Graphics-Quarta Simulator, Mentor Graphics-Precision RTL, Mentor Graphics Back End/Tanner Software tool, Mixed Signal simulator

**Hardware:** Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

